INPUT AND OUTPUT CIRCUIT OF SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

[0073] An input and output circuit of a semiconductor device is disclosed having an output buffer including first and second pull-up transistors connected in series between the power supply voltage and the pad, first and second pull-down transistors connected in series between the pad and the ground voltage, a pre-driver for pulling up or down a voltage of the pad when an output enable signal is enabled and for switching off the first and second pull-up transistors and the first and second pull-down transistors when the output enable signal is disabled, and a first circuit for adjusting voltage differences between respective gates and respective sources/drains of the first and second pull-up transistors and the first and second pull-down transistors to be below a predetermined voltage level in response to the first, second and third control signals under power on or power off conditions; and an input buffer including a transmission gate for transmitting an input signal applied to the pad to a first node in response to the first control signal, third, fourth and fifth pull-up transistors connected in series between the power supply voltage and a second node and having corresponding gates connected to a third node, the pad and the first node, respectively, a third pull-down transistor connected between the second node and the ground voltage and having a gate connected to the first node, a second circuit for adjusting voltage differences between respective gates and respective sources/drains of the third, fourth and fifth pull-up transistors and the third pull-down transistor to be below a predetermined voltage in response to the first and third control signals if the high voltage is applied to the pad under either power on or power off conditions.